Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-83. (Canceled)

84. (Currently Amended) A driving circuit comprising:

a shift register;

a first output enable signal line;

a second output enable signal line;

a video signal line;

a plurality of first NAND circuits, each of the plurality of first NAND circuits ~~electrically connecting~~ being electrically connected to the shift register, the each of the plurality of first NAND circuits ~~electrically connecting~~ being electrically connected to the first output enable signal line;

a plurality of second NAND circuits, each of the plurality of second NAND circuits ~~electrically connecting~~ being electrically connected to the shift register, the each of the plurality of second NAND circuits ~~electrically connecting~~ being electrically connected to the second output enable signal line;

a plurality of first analog switches ~~electrically connecting~~ being electrically connected to the video signal line, each of the plurality of first analog switches ~~electrically connecting~~ being electrically connected to one of the plurality of first NAND circuits; and

a plurality of second analog switches ~~electrically connecting~~ being electrically connected to the video signal line, each of the plurality of second analog switches ~~electrically connecting~~ being electrically connected to one of the plurality of second NAND circuits.

85. (Previously Presented) The driving circuit according to claim 84, the plurality of first NAND circuits and the plurality of second NAND circuits being arranged alternately.

86. (Currently Amended) An active matrix substrate comprising:

a plurality of scan lines;

a plurality of data lines crossing the scan lines; and

the driving circuit according to claim 84, the plurality of analog switches ~~electrically connecting~~ being electrically connected to the plurality of the data lines.

87. (Previously Presented) The active matrix substrate according to claim 86, the first output enable signal line outputting a first output enable signal, the second output enable signal line outputting a second output enable signal, wherein the second output enable signal line is to be set at a high level when the first output enable signal is to be set at a low level during a pulse generation period.

88. (Previously Presented) The active matrix substrate according to claim 86, the shift register having a plurality of stages, each of the plurality of stages being adapted to respond to one of a first clock signal and a second clock signal.

89. (Previously Presented) The active matrix substrate according to claim 88, wherein the first clock signal is to be set at a high level when the first output enable signal is to be set at a high level, and the first clock signal is to be set at a low level when the first output enable signal is to be set at a low level in a pulse generation period.

90. (Currently Amended) A display device, comprising:

a plurality of scan lines;

a plurality of data lines crossing the scan lines; and

the driving circuit according to claim 84, the plurality of analog switches ~~electrically connecting~~ being electrically connected to the plurality of the data lines.

91-93. (Canceled)

94. (Previously Presented) A driving circuit comprising:

a shift register;

a first output enable signal line;

a second output enable signal line;

a video signal line;

a plurality of first NAND circuits, each of the plurality of first NAND circuits controlled by a first output signal and a second output signal, the first output signal being outputted from the shift register, the second output signal being outputted from the first output enable signal line;

a plurality of second NAND circuits, each of the plurality of second NAND circuits controlled by a third output signal and a fourth output signal, the third output signal being outputted from the shift register, the fourth output signal being outputted from the second output enable signal line;

a plurality of first analog switches provided a video signal from the video signal line, each of the plurality of first analog switches being controlled by an output from one of the plurality of first NAND circuits; and

a plurality of second analog switches provided a video signal from the video signal line, each of the plurality of second analog switches being controlled by an output from one of the plurality of second NAND circuits.